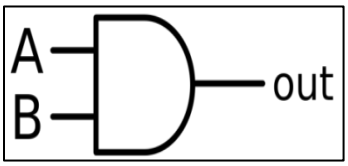
Practical-1

Aim: - To verify the Truth Table of Basic Logic Gates

APPARATUS REQUIRED: -Digital lab kit, single strand wires, breadboard, TTL IC's AND (IC-7408), OR (IC-7432), and NOT (IC-7404).

1) AND gate

The AND gate is an electronic circuit that gives a high output (1) only if all its inputs are high. A dot (.) is used to show the AND operation i.e. A.B or can be written as AB



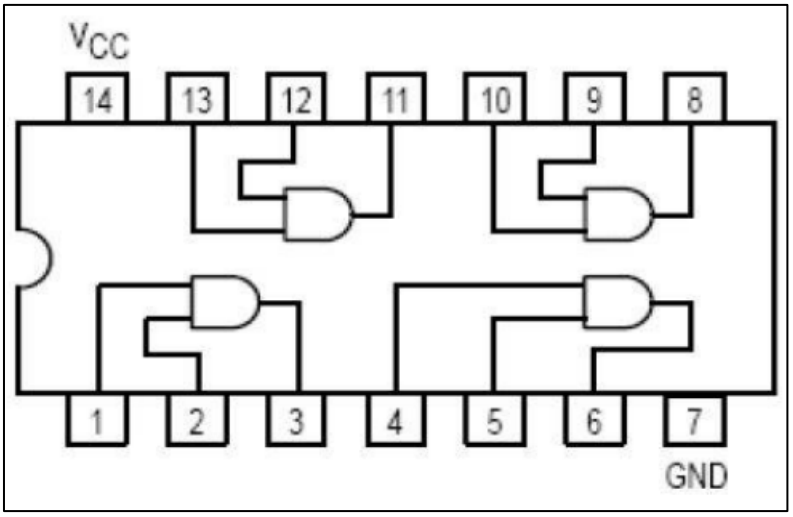
Y= A.B

Logic Symbol of AND Gate

A	B	Output
0	0	0
0	1	0
1	0	0
1	1	1

Truth Table:

Logic Circuit:-



2) OR gate

The OR gate is an electronic circuit that gives a high output (1) if one or more of its inputs are high. A plus (+) is used to show the OR operation.

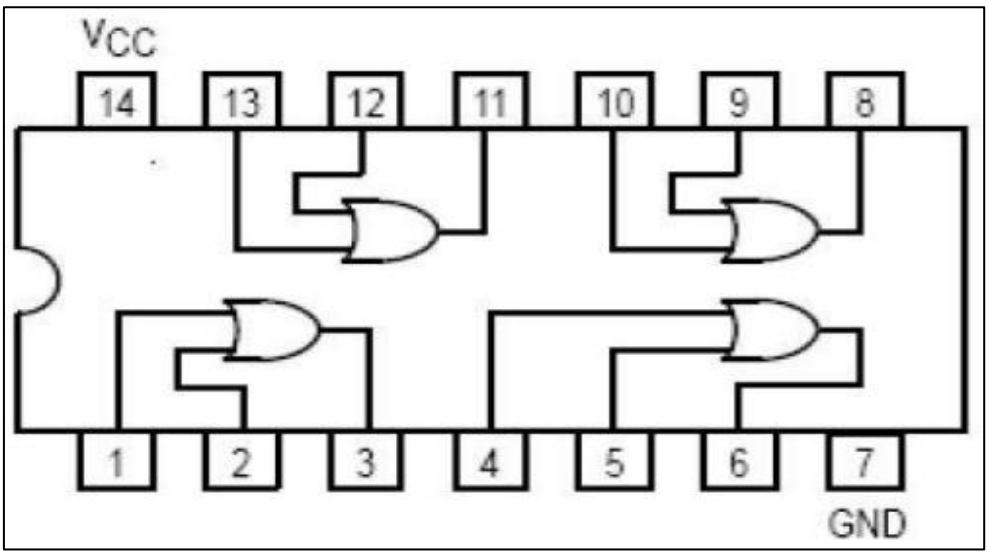
Y= A+B

Input		Output
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

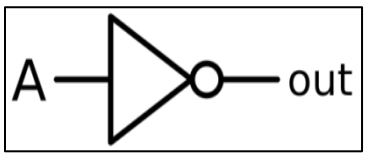
Logic Symbol of OR Gate

Truth Table:

Logic



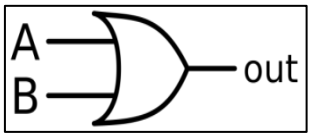
Circuit:-



1) **NOT gate**

The NOT gate is an electronic circuit that produces an inverted version of the input at its output. It is also known as an inverter. If the input variable is A, the inverted output is known as NOT A. This is also shown as A' or A with a bar over the top, as shown at the outputs.

Y= A'

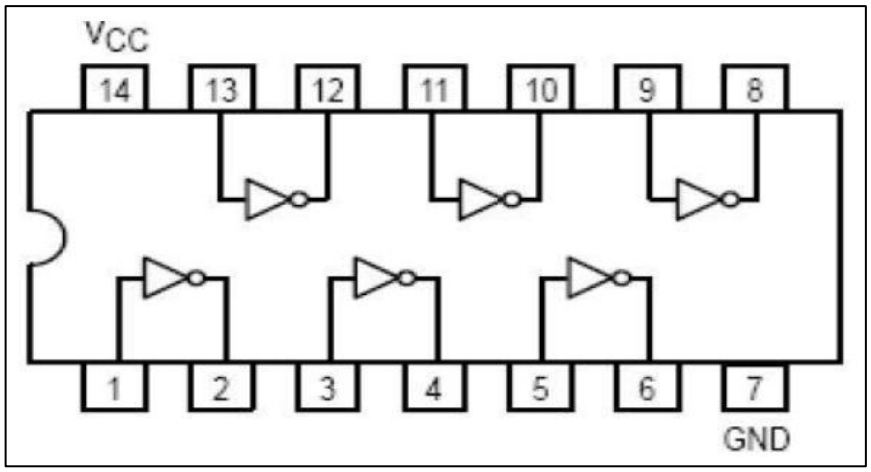


Logic Symbol of NOT Gate

Truth Table:

A	Output (~A)
0	1
1	0

Logic Circuit:-



Procedure:

1) Fix the I.C on the I.C trainer kit.
2) Connections are made as shown, using the pin details of the gates. Toggle switches and LED‟s in the trainer are used as inputs and outputs respectively.
3) = High or „1‟ state implies a voltage between 2.4V and 5.0V in the input state.

RESULT:

Thus the logic gates are studied and their truth tables were verified.

Practical-2

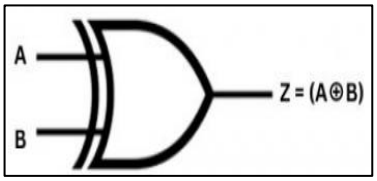
Aim: - To verify the Truth Table of Combinational Logic Gates
APPARATUS REQUIRED: lab kit, single strand wires, breadboard, IC's

Combinational Logic Circuits are made up from basic logic NAND, NOR or NOT gates that are "combined" or connected together to produce more complicated switching circuits. These logic gates are the building blocks of combinational logic circuits. An example of a combinational circuit is a decoder, which converts the binary code data present at its input into a number of different output lines, one at a time producing an equivalent decimal code at its output. Combinational logic circuits can be very simple or very complicated and any combinational circuit can be implemented with only NAND and NOR gates as these are classed as "universal" gates.

1) Ex-OR gate

The 'Exclusive-OR' gate is a circuit which will give a high output if either, but not both of its two inputs are high. An encircled plus sign (⊕) is used to show the Ex-OR operation.

Y=A⊕B

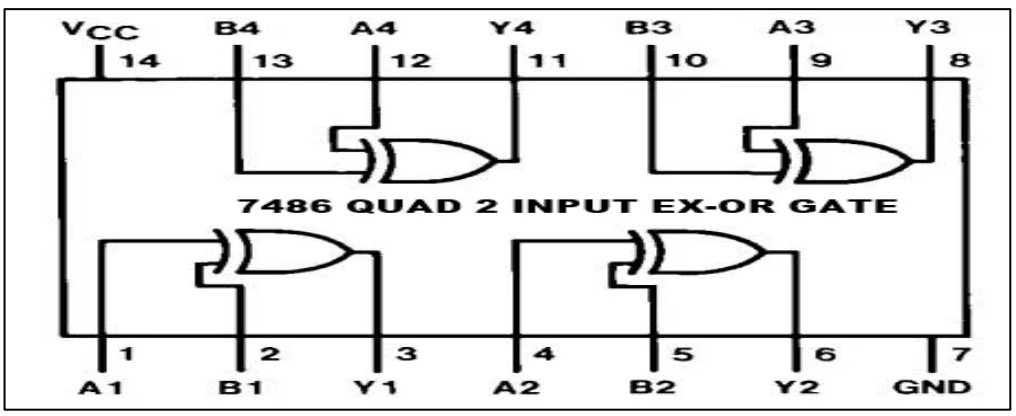


Logic Symbol Of Ex-OR gate

Truth Table of Ex-OR gate:-

A	B	A **XOR** B
0	0	0
0	1	1
1	0	1
1	1	0

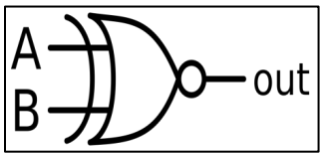
Logic Circuit of Ex-OR Gate:-



2) Ex-NOR gate

The 'Exclusive-NOR' gate circuit does the opposite to the EX-OR gate. It will give a low output if either, but not both of its two inputs are high. The symbol is an EX-OR gate with a small circle on the output. The small circle represents inversion.

Y= A⊕B

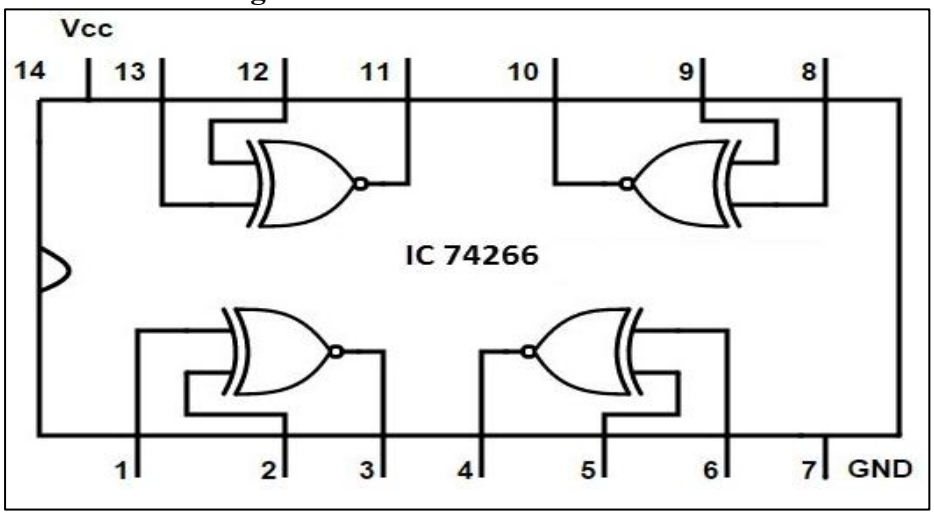


Logic Symbol of Ex-NOR gate

Truth Table of Ex-NOR gate:

A	B	Z=A⊙B
0	0	1
0	1	0
1	0	0
1	1	1

Logic circuit of EX-NOR gate:



PROCEDURE:

1. Connect the trainer kit to ac power supply.
2. Connect the NAND gates for any of the logic functions to be realized.
3. Connect the inputs of first stage to logic sources and output of the last gate to logic indicator.
4. Apply various input combinations and observe output for each one.
5. Verify the truth table for each input/ output combination.
6. Repeat the process for all logic functions. 7. Switch off the power supply.

RESULT:

Thus the logic gates are studied and their truth tables were verified.

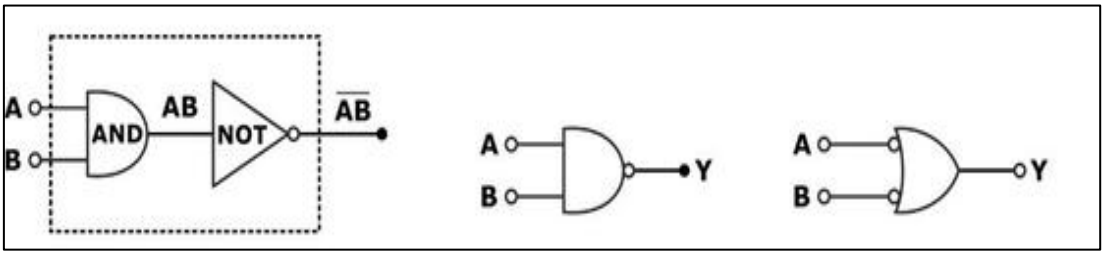
Practical-3

Aim: - To verify the Truth Table of Universal Logic Gates.

APPARATUS REQUIRED: - logic trainer kit, NAND gates (IC 7400), NOR gates (IC 7402), wires.

1) NAND Gate

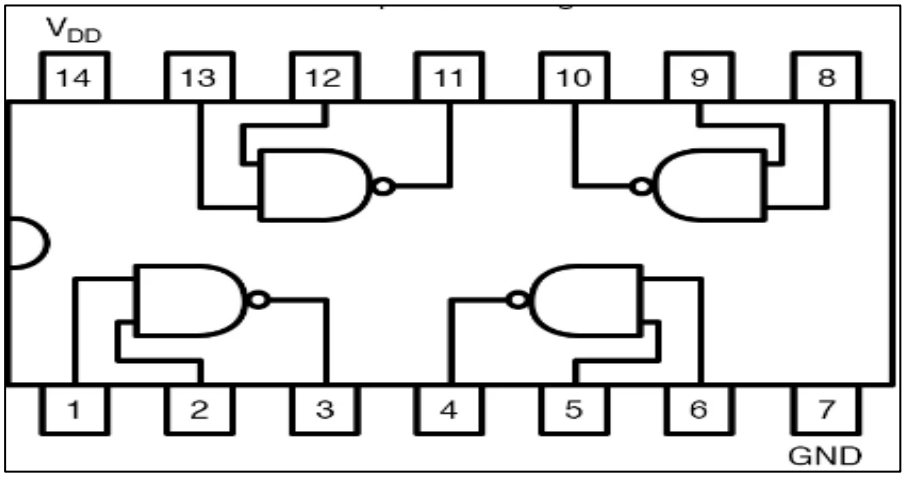
The NAND gate is one of the universal gates. The NAND gate is a AND gate followed by a NOT gate. Thus, we can say it is a AND NOT operation. It may have two or more inputs but only one output. The logical symbols of a NAND Gate and the truth table are shown below.



Truth Table:-

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

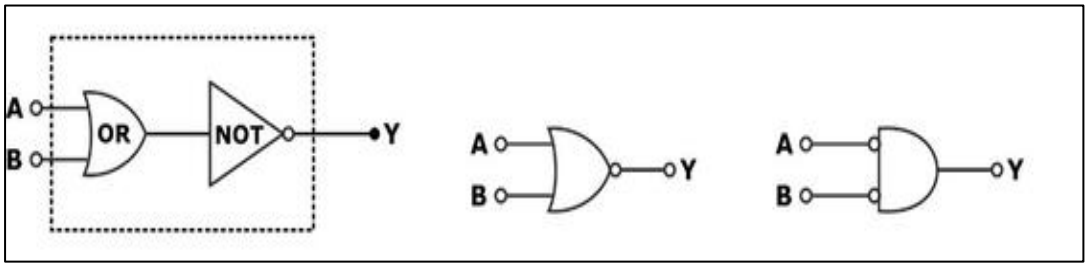
Logic Circuit:



2) NOR Gate

The NOR gate is one of the universal gates. A NOR gate combines two basic logic gates: an OR gate and a NOT gate. So we can say it is an OR-NOT operation. It may have two or more inputs and an output. The logical symbols of the NOR Gate are shown:

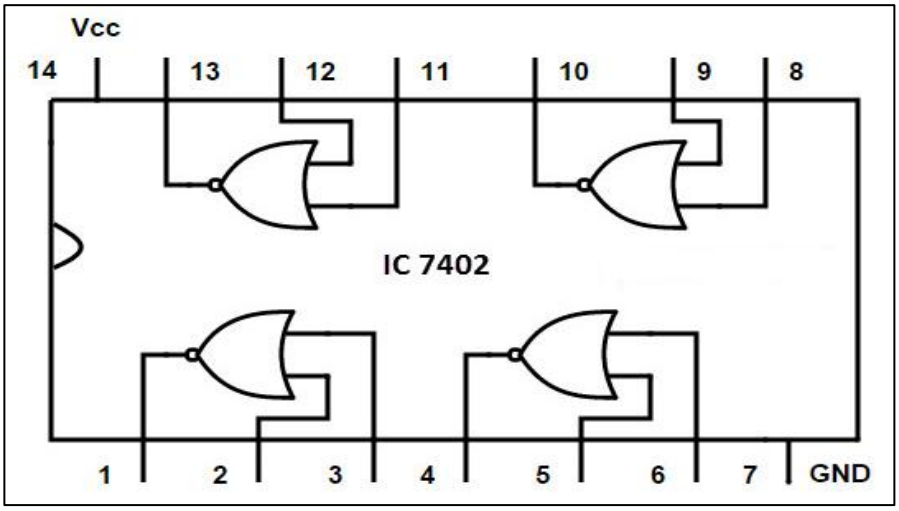
The logical expression for the output is



Truth Table:

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

Logic circuit:-



PROCEDURE:

1. Connect the trainer kit to ac power supply.
2. Connect the NOR gates for any of the logic functions to be realised.
3. Connect the inputs of first stage to logic sources and output of the last gate to logic indicator.
4. Apply various input combinations and observe output for each one.
5. Verify the truth table for each input/ output combination.
6. Repeat the process for all logic functions.
7. Switch off the ac power supply.

RESULT:

NAND & NOR are verified as universal gates successfully.

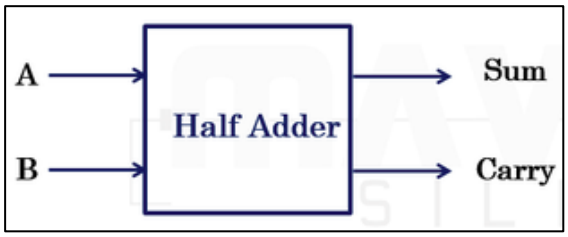
Practical-4

Aim:- To verify the Truth Table of Half Adder Combinational Circuit

APPARATUS REQUIRED: logic trainer kit, NAND gates (IC 7400), XOR gates (IC 7486), AND gates (IC 7408), wires.

Half Adder

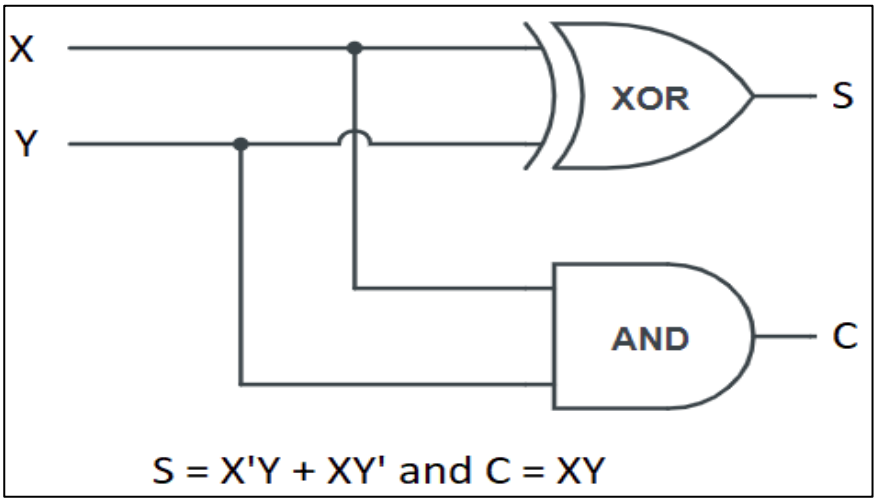
In the half adder circuit, first, two bits inputs are given to the half adder circuit and the circuit returns the sum of two bits and the carry as well. Let's see how the half adder circuit is formed.



Truth Table :

Inputs		Outputs	
A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Circuit Diagram of Half Adder:-



PROCEDURE:

(i) Connections are given as per circuit diagram.
(ii) Logical inputs are given as per circuit diagram.
(iii) Observe the output and verify the truth table.

RESULT:

Thus the half adder &full adder was designed and their truth table is verified.

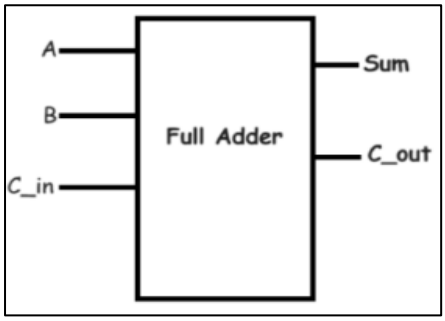
Practical-5

Aim:- To verify the Truth Table of Full Adder Combinational Circuit

APPARATUS REQUIRED: logic trainer kit, NAND gates (IC 7400), XOR gates (IC 7486), AND gates (IC 7408), wires.

Full Adder:-

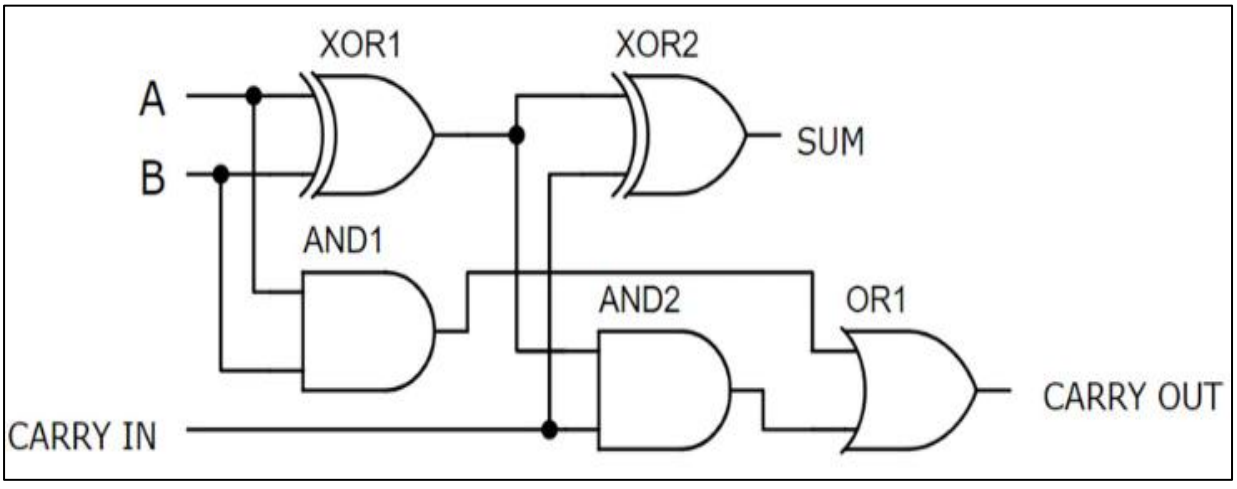
A combinational logic circuit that can add two binary digits (bits) and a carry bit, and produce a sum bit and a carry bit as output is known as a full-adder. In other words, a combinational circuit which is designed to add three binary digits and produces two outputs (sum and carry) is known as a full adder. Thus, a full adder circuit adds three binary digits, where two are the inputs and one is the carry forwarded from the previous addition. The block diagram and circuit diagram of the full adder are shown in below:-



Truth Table :-

Inputs			Outputs	
A	B	C_{in}	Carry	Sum
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Full Adder Logic Circuit :-



PROCEDURE:

(i) Connections are given as per circuit diagram.

(ii) Logical inputs are given as per circuit diagram.

(iii) Observe the output and verify the truth table.

RESULT:

Thus the half adder &full adder was designed and their truth table is verified.

Practical-6

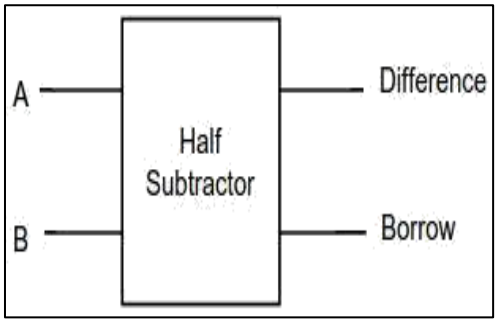
Aim:-To verify the Truth Table of Half Subtractor Combinational Circuit

APPARATUS REQUIRED: - logic trainer kit, NAND gates (IC 7400), XOR gates (IC 7486), AND gates (IC 7408), NOT gates (IC 7404), connecting wires.

Half Subtractor

The half-subtractor is a combinational circuit which is used to perform subtraction of two bits. It has two inputs, a (minuend) and B (subtrahend) and two outputs Difference and Borrow. The logic symbol and truth table are shown below.

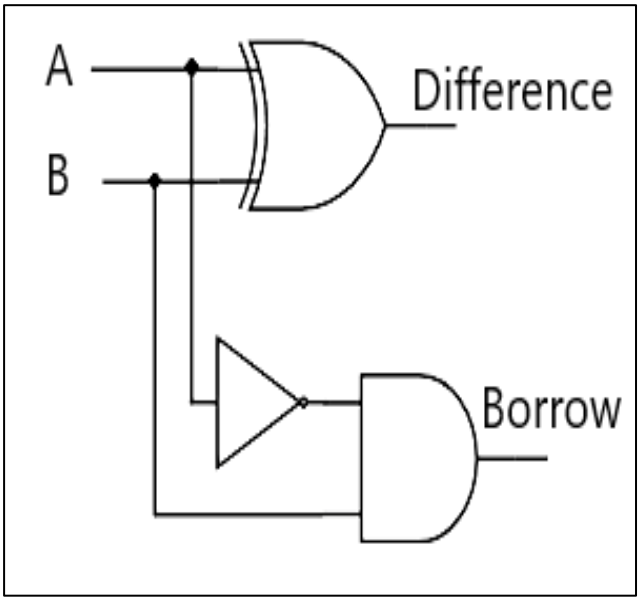
Logic Symbol of Half subtractor:-



Truth Table of Half subtractor:

Inputs		Outputs	
A	B	Difference	Borrow
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

Circuit Diagram of Half subtractor:-



PROCEDURE:

(i) Connections are given as per circuit diagram.

(ii) Logical inputs are given as per circuit diagram.

(iii) Observe the output and verify the truth table.

RESULT:

Thus the half subtractor was designed and their truth table is verified.

Practical-7

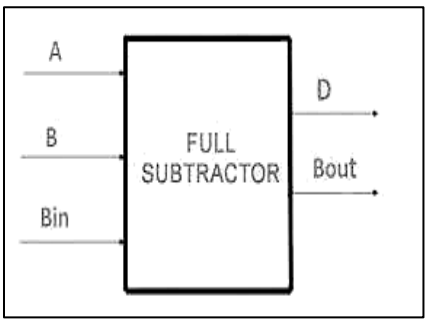
Aim:-To verify the Truth Table of Full Subtractor Combinational Circuit

APPARATUS REQUIRED: - logic trainer kit, NAND gates (IC 7400), XOR gates (IC 7486), AND gates (IC 7408), NOT gates (IC 7404), connecting wires.

Full Subtractor

A full subtractor is a combinational circuit that performs subtraction involving three bits, namely A (minuend), B (subtrahend), and Bin (borrow-in). It accepts three inputs: A (minuend), B (subtrahend) and a Bin (borrow bit) and it produces two outputs: D (difference) and Bout (borrow out). The logic symbol and truth table are shown below.

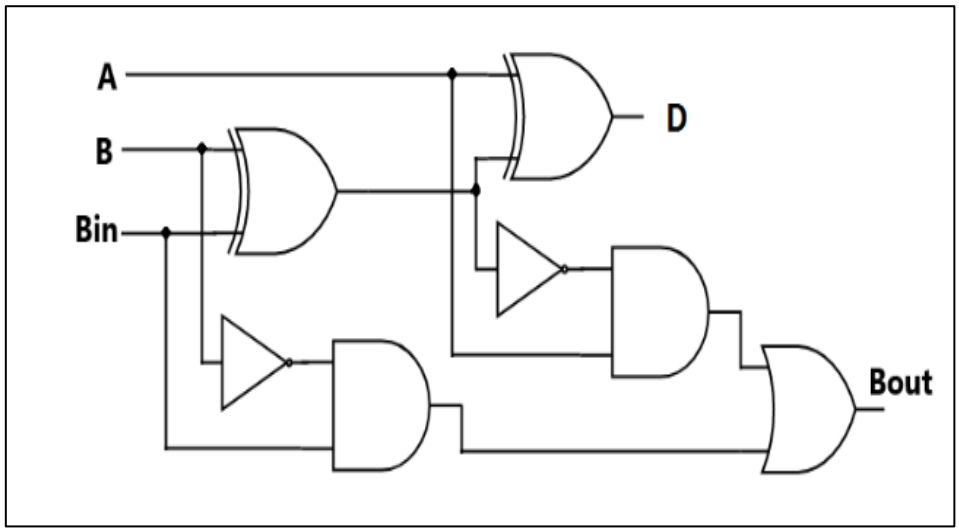
Logic Symbol of Full subtractor



Truth Table of Full subtractor

A	B	B_{in}	D	B_{out}
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Circuit Diagram of Full subtractor:



PROCEDURE:

(i) Connections are given as per circuit diagram.

(ii) Logical inputs are given as per circuit diagram.

(iii) Observe the output and verify the truth table.

RESULT:

Thus the full subtractor was designed and their truth table is verified.

Practical-8

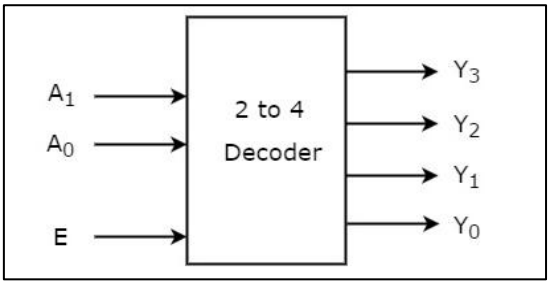
Aim:- To verify the Truth Table of Decoder Combinational Circuit

APPARATUS REQUIRED: - logic trainer kit, AND gates (IC 7408), NOT gates (IC 7404), connecting wires.

Decoder is a combinational circuit that has 'n' input lines and maximum of 2^n output lines. One of these outputs will be active High based on the combination of inputs present, when the decoder is enabled. That means decoder detects a particular code. The outputs of the decoder are nothing but the **min terms** of 'n' input variables lines, when it is enabled.

2 to 4 Decoder

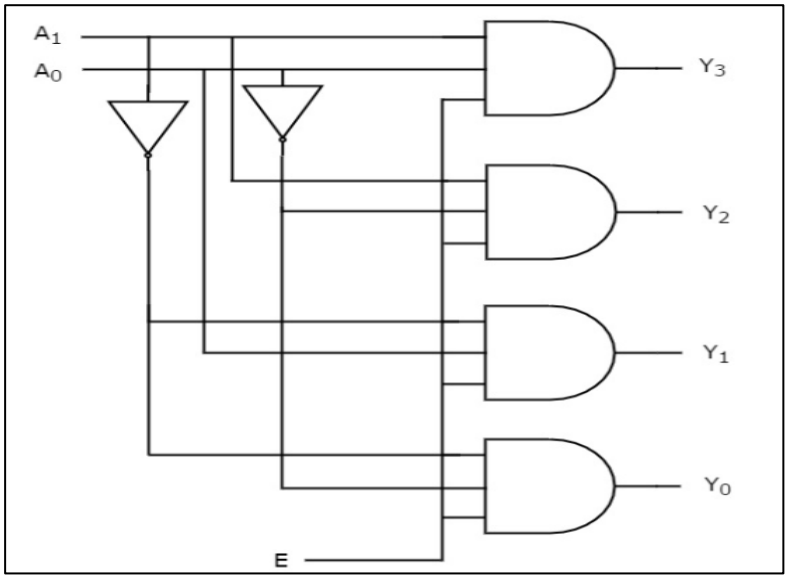
Let 2 to 4 Decoder has two inputs A_1 & A_0 and four outputs Y_3, Y_2, Y_1 & Y_0. The block diagram of 2 to 4 decoder is shown in the following figure.



Truth table:

Enable	INPUTS		OUTPUTS			
E	A_1	A_0	Y_3	Y_2	Y_1	Y_0
0	X	X	0	0	0	0
1	0	0	0	0	0	1
1	0	1	0	0	1	0
1	1	0	0	1	0	0
1	1	1	1	0	0	0

The circuit diagram of 2 to 4 decoder:-



PROCEDURE:

(i) Connections are given as per circuit diagram.

(ii) Logical inputs are given as per circuit diagram.

(iii) Observe the output and verify the truth table.

RESULT:

Thus the 2 to 4 Decoder was designed and their truth table is verified.

Practical-9

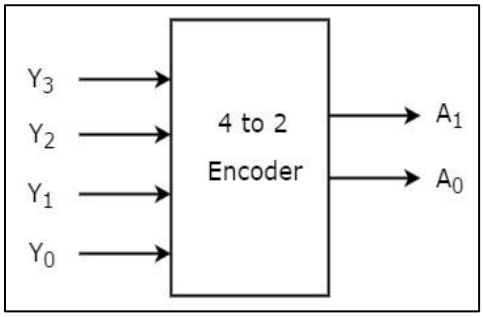
Aim:- To verify the Truth Table of Encoder Combinational Circuit

APPARATUS REQUIRED: - logic trainer kit, OR gate (IC-7432), connecting wires.

An **Encoder** is a combinational circuit that performs the reverse operation of Decoder. It has maximum of 2^n input lines and 'n' output lines. It will produce a binary code equivalent to the input, which is active High. Therefore, the encoder encodes 2^n input lines with 'n' bits. It is optional to represent the enable signal in encoders.

4 to 2 Encoder

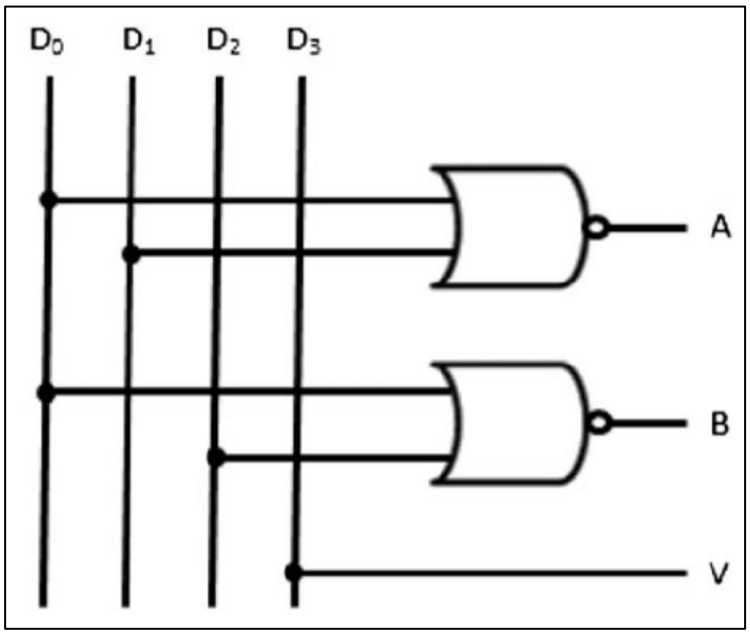
Let 4 to 2 Encoder has four inputs Y_3, Y_2, Y_1 & Y_0 and two outputs A_1 & A_0. The block diagram of 4 to 2 Encoder is shown in the following figure.



Truth Table:

INPUTS				OUTPUTS	
Y_3	Y_2	Y_1	Y_0	A_1	A_0
1	0	0	0	0	0
0	1	0	0	0	1
0	0	1	0	1	0
0	0	0	1	1	1

Logical circuit of the above expressions is given below:



PROCEDURE:

(i) Connections are given as per circuit diagram.

(ii) Logical inputs are given as per circuit diagram.

(iii) Observe the output and verify the truth table.

RESULT:

Thus the 4 to 2 encoder was designed and their truth table is verified.

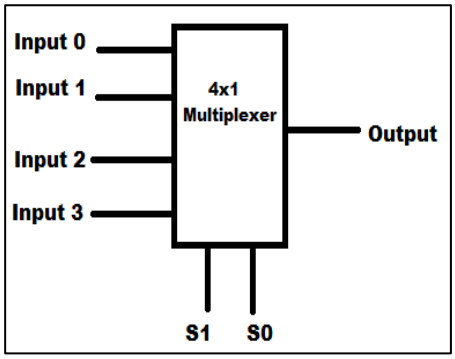
Practical-10

Aim:- To verify the Truth Table of Multiplexer Combinational Circuit
APPARATUS REQUIRED: - logic trainer kit, IC- 74150, wires.

MULTIPLEXER: Multiplexer generally means many into one. A multiplexer is a circuit with many inputs but only one output. By applying control signals we can steer any input to the output. The circuit has n-input signal, control signal (m) & one output signal, where $2^n=m$. One of the popular multiplexers is the 16 to 1 multiplexer, which has 16 input bits, 4 control bits & 1 output bit.

4x1 Multiplexer

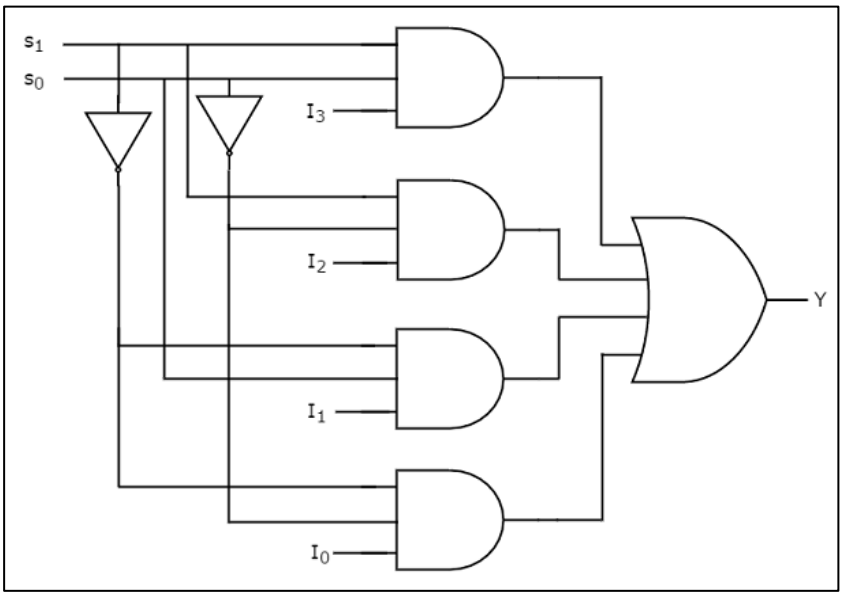
The 4x1 Multiplexer has four input lines I0, I1, I2 and I3 and one output line Y. The selection of a particular input is controlled by set of selection lines, S_1 and S_0.



Truth Table:-

INPUTS		Output
S_1	S_0	Y
0	0	A_0
0	1	A_1
1	0	A_2
1	1	A_3

The circuit diagram Multiplexer:-



PROCEDURE: -

1) Assemble the circuit on bread board, as per above diagram.
2) Give the logical inputs and check for the proper output, as per the truth table.

RESULT:

Hence verified the Multiplexer (8:1) operation using IC-74150.

Practical-11

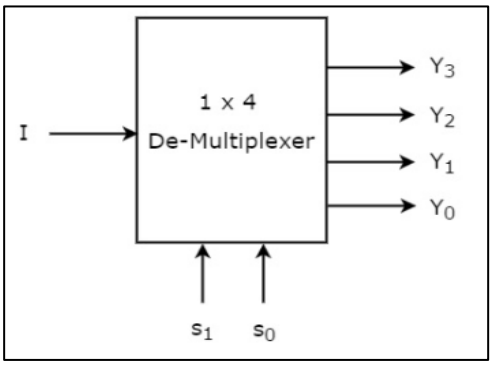
Aim: - To verify the Truth Table of De Multiplexer Combinational Circuit

APPARATUS REQUIRED: - Logic trainer kit, IC- 74154, wires.

De-Multiplexer is a combinational circuit that performs the reverse operation of Multiplexer. It has single input, 'n' selection lines and maximum of 2^n outputs. The input will be connected to one of these outputs based on the values of selection lines. Since there are 'n' selection lines, there will be 2^n possible combinations of zeros and ones. So, each combination can select only one output. De-Multiplexer is also called as **De-Mux**.

1x4 De-Multiplexer

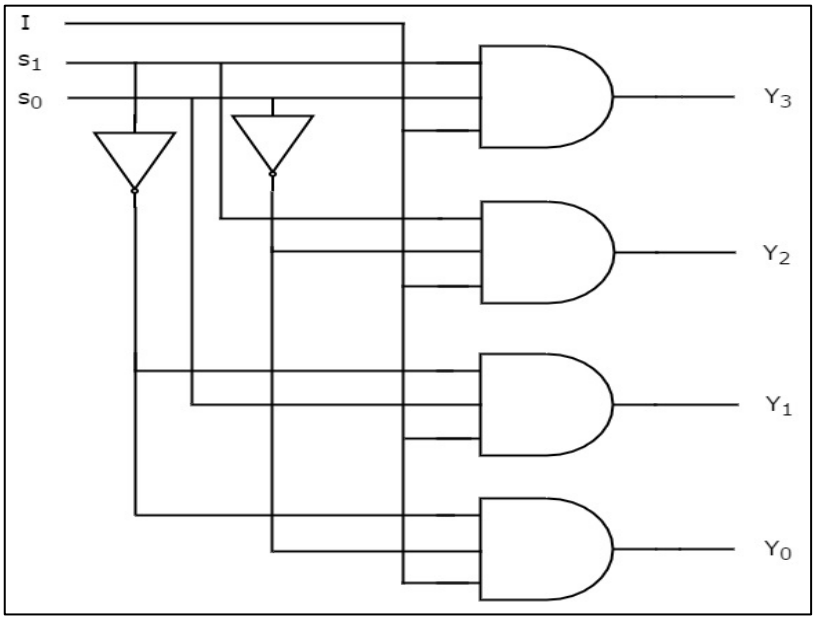
1x4 De-Multiplexer has one input I, two selection lines, s_1 & s_0 and four outputs Y_3, Y_2, Y1 &Y_0. The block diagram of 1x4 De-Multiplexer is shown in the following figure.



Truth Table:-

INPUTS		Output			
S_1	S_0	Y_3	Y_2	Y_1	Y_0
0	0	0	0	0	A
0	1	0	0	A	0
1	0	0	A	0	0
1	1	A	0	0	0

The circuit diagram De - Multiplexer:-



PROCEDURE: -

1) Assemble the circuit on bread board, as per above Pin diagram.
2) Give the logical inputs and check for the proper output, as per the truth table.

RESULT:

Hence verified the De-multiplexer (16:1) operation using IC-74154.