Practical-12

Aim: - To verify the Truth Table of S-R Flip-Flop

APPARATUS REQUIRED: - Logic trainer kit, IC 7400, wires.

S-R Flip Flop

It is a Flip Flop with two inputs, one is S and other is R. **S** here stands for Set and **R** here stands for Reset. Set basically indicates set the flip flop which means output 1 and reset indicates resetting the flip flop which means output 0. Here clock pulse is supplied to operate this flip flop, hence it is clocked flip flop.

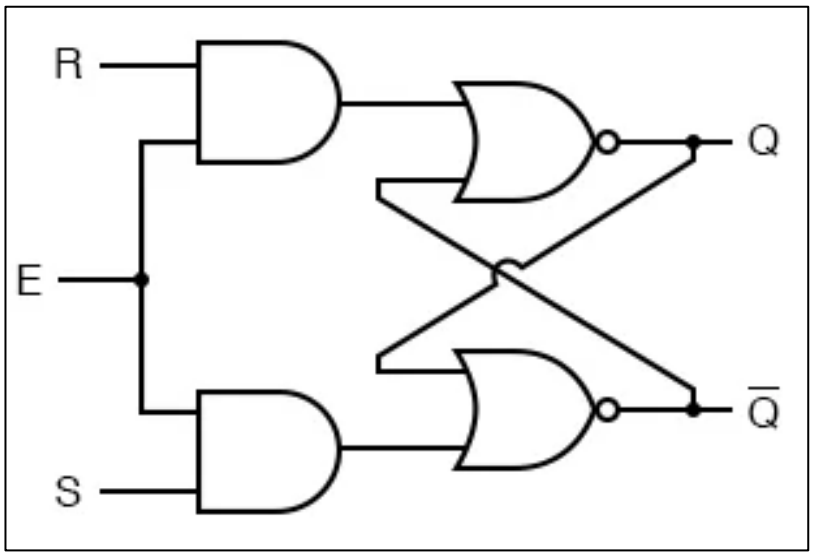
Working of SR Flip Flop

- **Case 1**: Let's say, **S=0** and **R=0**, then output of both AND gates will be 0 and the value of Q and Q' will be same as their previous value, i.e., Hold state.
- **Case 2**: Let's say, **S=0 and R=1**, then output of both AND gates will be 1 and 0, correspondingly the value of Q will be 0 as one of input is 1 and it is a NOR gate so it will ultimately give 0, hence Q gets 0 value, similarly Q' will be 1.
- **Case 3**: Let's say, **S=1 and R=0**, then output of both AND gates will be 0 and 1, correspondingly the value of Q' will be 0 as one of input to NOR gate is 1, so output will be 0 ultimately and this 0 value will go as input to upper NOR gate, and hence Q will become 1.
- **Case 4**: Let's say, **S=1 and R=1**, then output of both AND gates will be 1 and 1 which is invalid, as the outputs should be complement of each other.

Truth Table:-

S	R	Q	Q`
0	0	0	1
0	1	0	1
1	0	1	0
1	1	∞	∞

Circuit diagram:-



PROCEDURE: -

1. Connect the circuit as shown in figure.
2. Apply VCC & ground signal to the IC.
3. Observe the input & output according to the truth table.

Result:-

The observation table S-R Flip-Flops is verified.

Practical-13

Aim: - To verify the Truth Table of J-K Flip-Flop

APPARATUS REQUIRED: - Logic trainer kit, Flip-flop ICs- 7476, wires.

J-K Flip-Flop

K flip flop operates on sequential logic principle, where the output is dependent not only on the current inputs but also on the previous state. There are two inputs in JK Flip Flop Set and Reset denoted by J and K. It also has two outputs Output and complement of Output denoted by Q and $\overline{Q}$. The internal circuitry of a JK Flip Flop consists of a combination of logic gates, usually NAND gates.

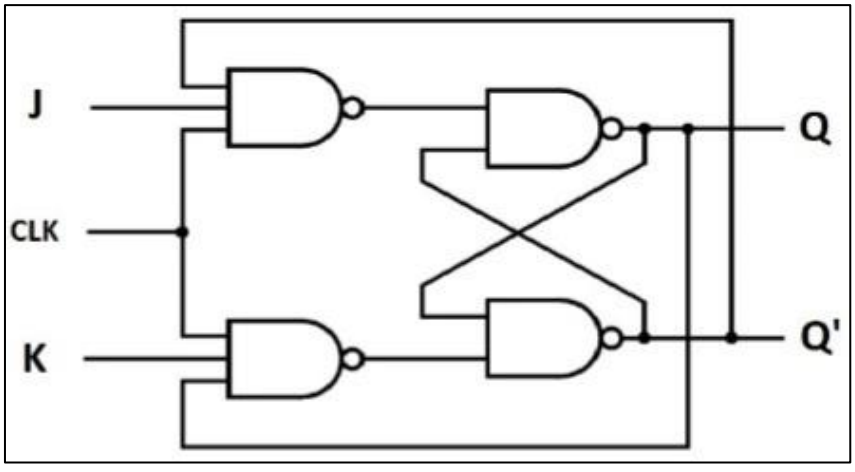
JK flip flop comprises four possible combinations of inputs: J=0, K=0; J=0, K=1; J=1, K=0; and J=1, K=1. These input combinations determine the behaviour of flip flop and its output.

- J=0, K=0: In this state, flip flop retains its preceding state. It neither sets nor resets itself, making it stable.
- J=0, K=1: This input combination forces flip flop to reset, resulting in Q=0 and $\overline{Q}$=1. It is often referred to as the "reset" state.
- J=1, K=0: Here, flip flop resides in the set mode, causing Q=1 and $\overline{Q}$=0. It is known as the "set" state.
- J=1, K=1: This combination toggles flip flop. If the previous state is Q=0, it switches to Q=1 and vice versa. This makes it valuable for frequency division and data storage applications.

Truth Table:-

Truth Table			
Q	J	K	Q(t+1)
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

Circuit diagram:-



PROCEDURE:

1) Connections are given as per circuit diagram.
2) Logical inputs are given as per circuit diagram.
3) Observe the output and verify the truth table.

RESULT: Thus the J-K Flip flop was designed and truth table is verified.

Practical-14

Aim: - To verify the Truth Table of Master Slave J-K Flip-Flop

APPARATUS REQUIRED: - Logic trainer kit, Flip-flop ICs- 7476, wires.

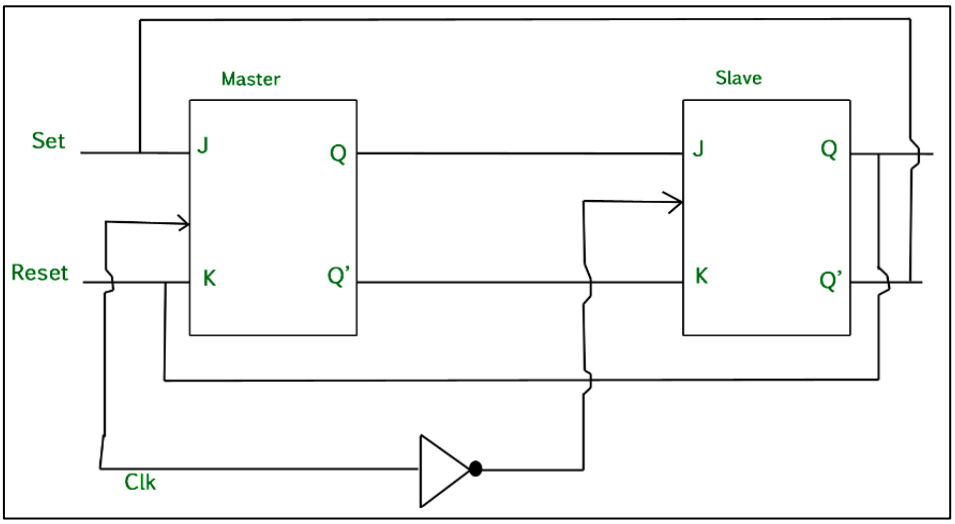
Master Slave J-K Flip-Flop

A **JK flip flop** is a type of 1-bit memory element having inputs namely J and K, one clock input, and two output specified by Q and Q'. The JK flip flop is an improved version of SR flip flop which does not have forbidden state. To avoid the forbidden or indeterminate state, the outputs of the JK flip flop are fed back to its inputs.

However, due to these feedback paths, a new problem is raised in the circuit, which is called race around condition. Race around condition in the JK flip is a major problem in which the outputs of flip flop are toggled continuously till the end of applied clock signal.

To avoid the problem of race around condition in JK flip flop, we use the JK flip flop in the **Master and Slave Mode**. Hence, the JK flip flop is called **Master-Slave Flip Flop**.

Master-Slave JK Flip Flop



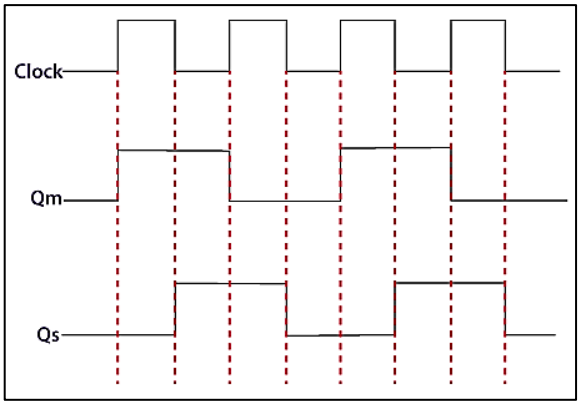
Working of a master slave flip flop –

1. When the clock pulse goes to 1, the slave is isolated; J and K inputs may affect the state of the system. The slave flip-flop is isolated until the CP goes to 0. When the CP goes back to 0, information is passed from the master flip-flop to the slave and output is obtained.
2. Firstly the master flip flop is positive level triggered and the slave flip flop is negative level triggered, so the master responds before the slave.
3. If J=0 and K=1, the high Q' output of the master goes to the K input of the slave and the clock forces the slave to reset, thus the slave copies the master.
4. If J=1 and K=0, the high Q output of the master goes to the J input of the slave and the Negative transition of the clock sets the slave, copying the master.
5. If J=1 and K=1, it toggles on the positive transition of the clock and thus the slave toggles on the negative transition of the clock.
6. If J=0 and K=0, the flip flop is disabled and Q remains unchanged.

Truth Table:-

Inputs				Output
J	K	Q_n	$Q_{(n+1)}$	D
0	0	0	0	0
0	0	1	1	1
0	1	0	0	0
0	1	1	0	0
1	0	0	1	1
1	0	1	1	1
1	1	0	1	1
1	1	1	0	0

Timing Diagram of a Master Flip Flop:



PROCEDURE:

1) Connections are given as per circuit diagram.
2) Logical inputs are given as per circuit diagram.
3) Observe the output and verify the truth table.

RESULT: Thus the Master slave J-K Flip flop was designed and truth table is verified.

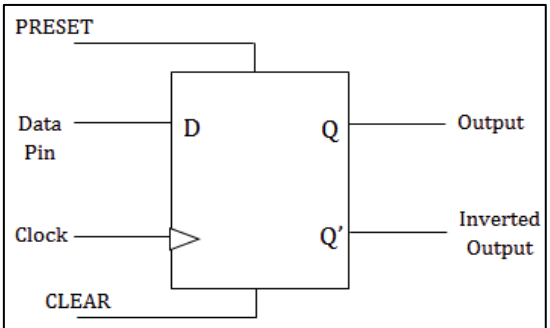
Practical-15

Aim: - To verify the Truth Table of D Flip-Flop

APPARATUS REQUIRED: - Logic trainer kit, Flip-flop ICs- 7474, wires.

D flip flop

D flip flop also called as delay flip flop where it can be used to introduce a delay in the digital circuit by changing the propagation delay of the flip flop. Here the input data bit at D will reflects at the output after a certain propagation delay.



Symbol: D Flip-flop

Truth Table:-

Truth Table of D Flip-Flop				Characteristic Table of D Flip-Flop		
Clock	INPUT	OUTPUT		D	Q	Q'
	D	Q	0	0	0	**0**
LOW	X	0	0	1	0	0
HIGH	0	0	1	0	1	1
HIGH	1	1	1	1	1	1

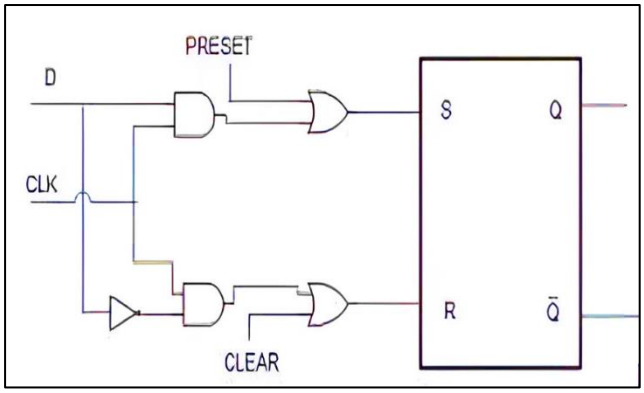
Characteristic Equation:

$$Q' = D\,Q' + D\,Q$$
$$Q' = D$$

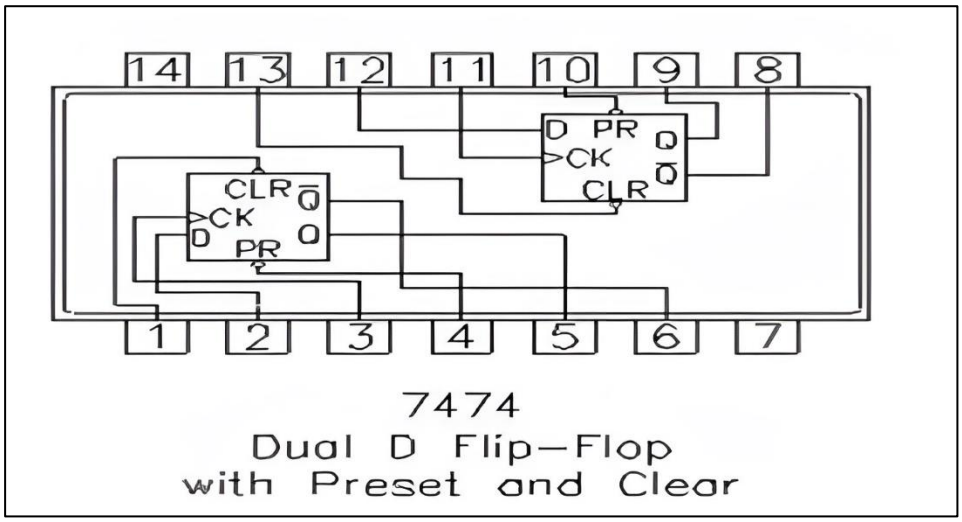
D Flip Flop with PRESET and CLEAR

PRESET is the input to the D flip flop which sets the output data to High i.e. 1. And CLEAR is also an input which clears the output data or output state. A high PRESET forces Q to 1; a high CLEAR resets Q to 0. Figure shows clocked flip flop with PRESET and CLEAR inputs.

Clocked D Flip-Flop with PRESET and CLEAR



Circuit diagram:-



PROCEDURE:

(i) Connections are given as per circuit diagram.
(ii) Logical inputs are given as per circuit diagram.
(iii) Observe the output and verify the truth table.

RESULT: Thus the D Flip flop was designed and their truth table is verified.

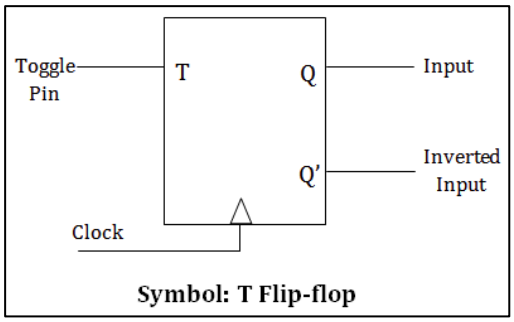
Practical-16

Aim: - To verify the Truth Table of T Flip-Flop.

APPARATUS REQUIRED: - Logic trainer kit, Flip-flop ICs-7400, 7404, 7410, wires.

T flip flop

T flip flop is similar to JK flip flop. Just tie both J and K inputs together to get a T Flip flop. Just like the D flip flop, it has only one external input along with a clock.



Symbol: T Flip-flop

T Flip-Flop Working:

Let us take a look at the possible cases and write it down in our truth table. The clock is always 1, so only two cases are possible where T can be high or low.

Case 1: T=0

Gate1 = 0, Gate2 = 0, Gate3/Q(n+1) = Q, Gate4/Q(n+1)' = Q'

Note:

- Since one of the inputs to Gate1 and gate2 is 0 and both are AND gates; the output of gate1 and gate2 will be equal to 0 irrespective of other inputs as per the property of AND gates
- Gate3 = (0+Q')' = (Q')' = Q
- Gate4 = (0+Q)' = (Q)' = Q'

Case 2: T=1

Gate1 = Q, Gate2 = Q', Gate4/Q (n+1)' = 0, Gate3/Q(n+1) = Q'

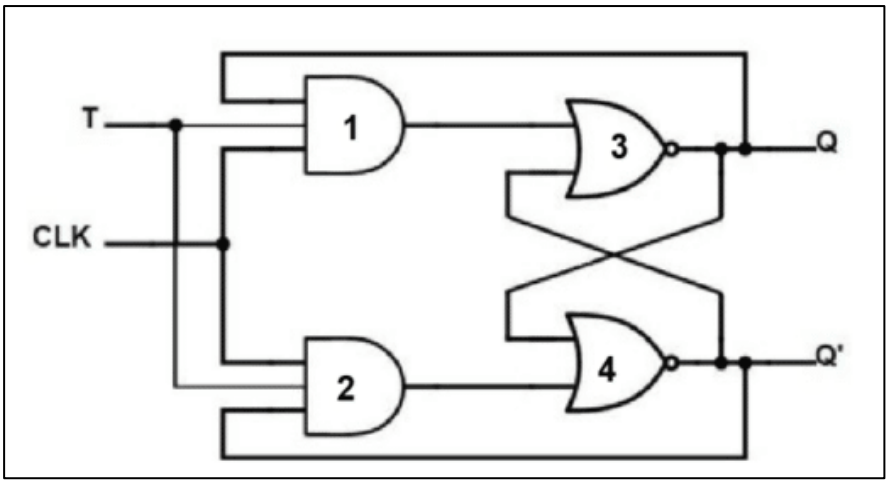
Note:

- Since one input of both gate1 and gate2 is 0 and both gates are AND gates, the output of both gates will be equal to the third input.
- Gate4 = (Q'+Q)' = 1' = 0
- Gate3 = (Q+0)' = Q'

T Flip-Flop Truth Table:

T	Q_n	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

Circuit diagram:-



PROCEDURE:

(i) Connections are given as per circuit diagram.
(ii) Logical inputs are given as per circuit diagram.
(iii) Observe the output and verify the truth table.

RESULT: Thus the T Flip flop was designed and their truth table is verified.

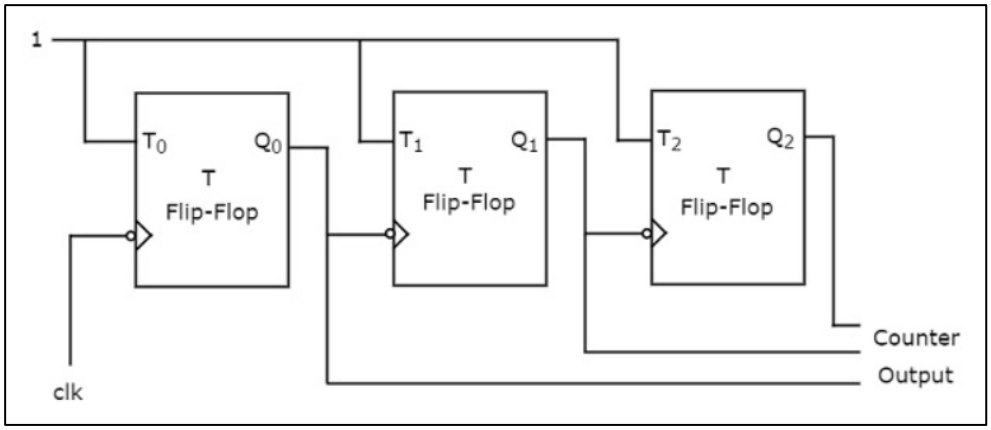
Practical-17

Aim: - To verify the working of Asynchronous up Counter.

APPARATUS REQUIRED: Logic trainer kit, Flip-flop ICs-7400, 7404, 7410, Resistor 220Ω, Battery 9V, wires.

Asynchronous up Counter

An 'N' bit binary counter consists of 'N' T flip-flops. If the counter counts from 0 to $2^N - 1$, then it is called as binary **up counter**. The **block diagram** of 3-bit Asynchronous binary up counter is shown in the following figure.



The 3-bit Asynchronous binary up counter contains three T flip-flops and the T-input of all the flip-flops are connected to '1'. All these flip-flops are negative edge triggered but the outputs change asynchronously. The clock signal is directly applied to the first T flip-flop. So, the output of first T flip-flop **toggles** for every negative edge of clock signal.

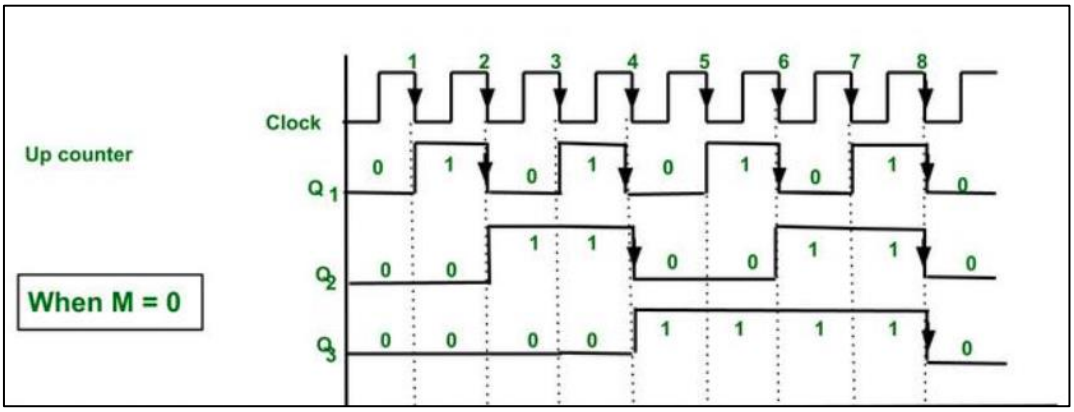
The output of first T flip-flop is applied as clock signal for second T flip-flop. So, the output of second T flip-flop toggles for every negative edge of output of first T flip-flop. Similarly, the output of third T flip-flop toggles for every negative edge of output of second T flip-flop, since the output of second T flip-flop acts as the clock signal for third T flip-flop.

Assume the initial status of T flip-flops from rightmost to leftmost is Q2Q1Q0=000 Here, Q2 & Q0 are MSB & LSB respectively. We can understand the **working** of 3-bit asynchronous binary counter from the following table.

Truth Table:

3-bit Asynchronous up counter			
Clock	**Q_C**	**Q_B**	**Q_A**
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

Timing diagram:



When M=0, then M' =1.
Put this in Y= **M'Q + MQ'= Q** So Q is acting as clock for next FFs.
Therefore, the counter will act as Up counter.

Explanation of up counter –

- The 1st FF is connected to logic 1. Therefore, it will toggle for every falling edge.
- The 2nd FF input is connected to Q_1.Therefore it changes its state when Q_1= 1 and there is falling edge of clock.
- Similarly, 3rd FF is connected to Q_2. Therefore, it changes its state when Q_2= 1 and there is falling edge of clock.
- By this we can generate counting states of up counter.
- After every 8th falling edge the counter is again reaching to state 0 0 0.
  Therefore, it is also known as divide by 8 circuit or mod 8 counter.

PROCEDURE: -

1. Connect the circuit as shown in figure.
2. Apply VCC & ground signal to the IC.
3. Apply various input data to the logic circuit.
4. Observe the input & output according to the truth table.

RESULT: - The 3-bit binary asynchronous up counter is verified.

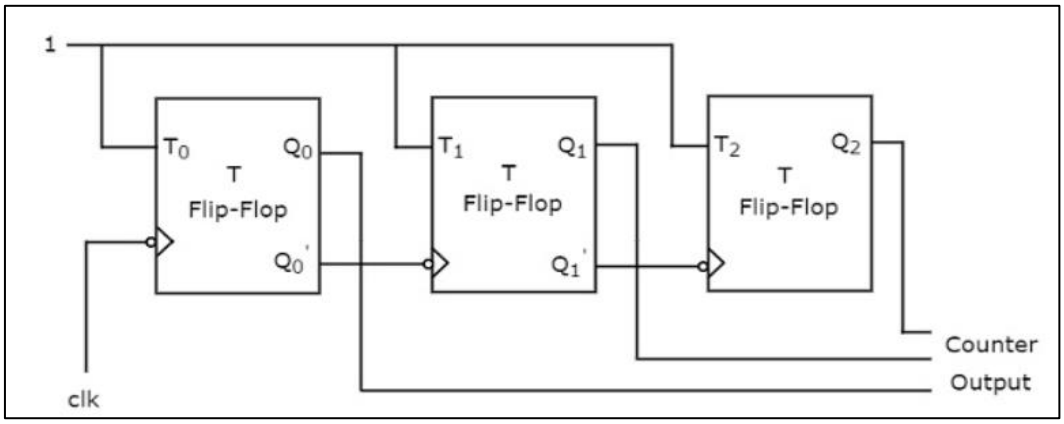
Practical-18

Aim: - To verify the working of Asynchronous down Counter.

APPARATUS REQUIRED: Logic trainer kit, Flip-flop ICs-7400, 7404, 7410, Resistor 220Ω, Battery 9V, wires.

Asynchronous down Counter

An 'N' bit Asynchronous binary down counter consists of 'N' T flip-flops. It counts from $2^N - 1$ to 0. The **block diagram** of 3-bit Asynchronous binary down counter is shown in the following figure.



The block diagram of 3-bit Asynchronous binary down counter is similar to the block diagram of 3-bit Asynchronous binary up counter. But, the only difference is that instead of connecting the normal outputs of one stage flip-flop as clock signal for next stage flip-flop, connect the **complemented outputs** of one stage flip-flop as clock signal for next stage flip-flop. Complemented output goes from 1 to 0 is same as the normal output goes from 0 to 1.

Assume the initial status of T flip-flops from rightmost to leftmost is Q2Q1Q0=000Here, Q2 & Q0 are MSB & LSB respectively. We can understand the **working** of 3-bit asynchronous binary down counter from the following table.

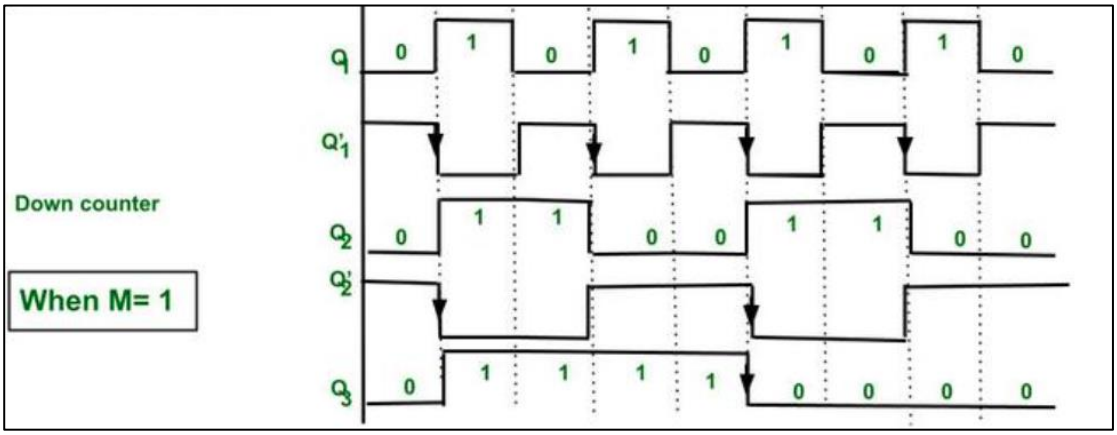
Truth Table:

Counter State	Q_2	Q_1	Q_0
7	1	1	1
6	1	1	0
5	1	0	1
4	1	0	0
3	0	1	1
2	0	1	0
1	0	0	1
0	0	0	0

Here Q0toggled for every negative edge of clock signal. Q1 toggled for every Q0that goes from 0 to 1, otherwise remained in the previous state. Similarly, Q2toggled for every Q1that goes from 0 to 1, otherwise remained in the previous state.

The initial status of the T flip-flops in the absence of clock signal is Q2Q1Q0=000This is decremented by one for every negative edge of clock signal and reaches to the same value at 8th negative edge of clock signal. This pattern repeats when further negative edges of clock signal are applied.

Timing diagram:



When M=1, then M' =0.
Put this in **Y= M'Q + MQ'= Q'**. So Q' is acting as clock for next FFs.
Therefore, the counter will act as Down counter.

Explanation of down counter

- The 1st FF is connected to logic 1. Therefore, it will toggle for every falling edge.
- The 2nd FF input is connected to Q'1.Therefore it changes its state when Q'1= 1 and there is falling edge of clock.
- Similarly, 3rd FF is connected to Q'2. Therefore, it changes its state when Q'2= 1 and there is falling edge of clock.
- By this we can generate counting states of down counter.
- After every 8th falling edge the counter is again reaching to state 0 0 0.
- Therefore, it is also known as divide by 8 circuit or mod 8 counter.

PROCEDURE: -
1. Connect the circuit as shown in figure.
2. Apply VCC & ground signal to the IC.
3. Apply various input data to the logic circuit.
4. Observe the input & output according to the truth table.

RESULT: - The 3-bit binary asynchronous down counter is verified.

Practical-19

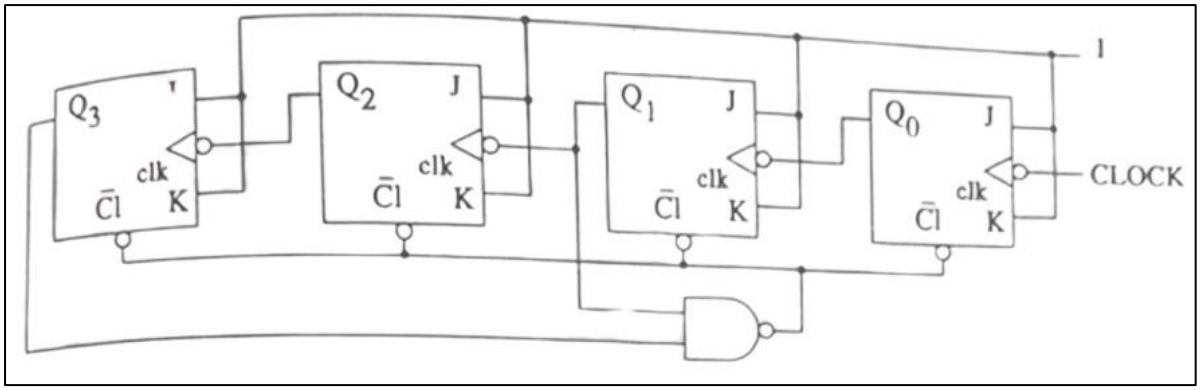
Aim: - To verify the working of Asynchronous MOD-N Counter

APPARATUS REQUIRED: Trainer Kit, IC 7490, IC 7400, and IC 7410, Patch chord.

Asynchronous MOD-N Counter

A mod-W (or divide-by-N) asynchronous counter, where N=T, will count up to (N- 1) (an output of all 1's) before resetting to all 0*s and beginning the count sequence again.

A general mod-N counter can be produced by using flip-flops with clear inputs and then simply decoding the nth count state and using this to reset all flip-flops to zero. The count will therefore be from 0 to (TV-1) repeated since the circuit resets when the count gets to N. Note that because the Nth state must exist before it can be used to reset all of the flip-flops there is the likelihood that glitches will occur in some of the output lines during the resetting phase (since an output may go high as the reset count is reached, and then be reset to 0).



Truth Table:

Reset all flip-flops	$\bar{Q}_3\bar{Q}_2$	$\bar{Q}_3Q_2$	Q_3Q_2	$Q_3\bar{Q}_2$
$\bar{Q}_1\bar{Q}_0$	0	0	x	0
$\bar{Q}_1Q_0$	0	0	x	0
Q_1Q_0	0	0	x	x
$Q_1\bar{Q}_0$	0	0	x	1

RESULT: Thus the Mod-N Counter is constructed and verified.

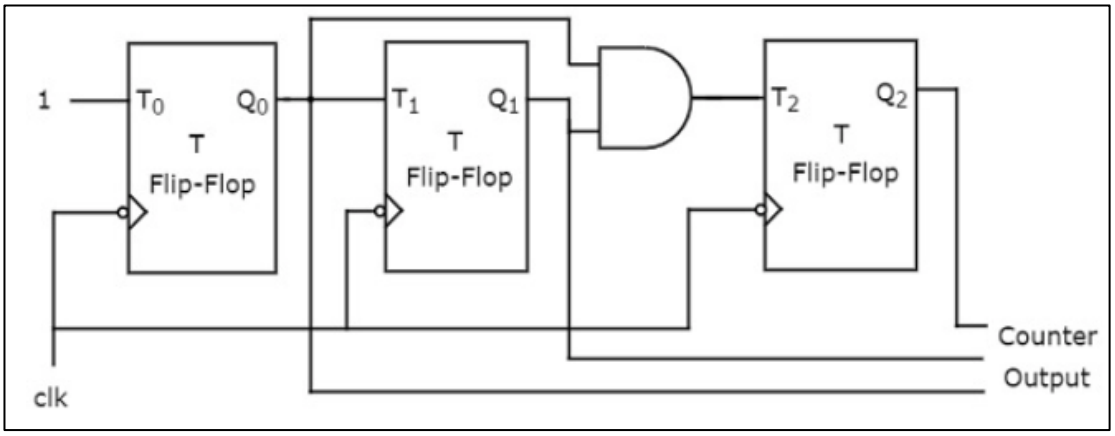
Practical-20

Aim: - To verify the working of Synchronous up Counter

APPARATUS REQUIRED: Logic trainer kit, Flip-flop ICs-7400, 7404, 7410, Resistor 220Ω, Battery 9V, wires.

Synchronous Binary up Counter:

An 'N' bit Synchronous binary up counter consists of 'N' T flip-flops. It counts from 0 to $2^N - 1$. The **block diagram** of 3-bit Synchronous binary up counter is shown in the following figure.



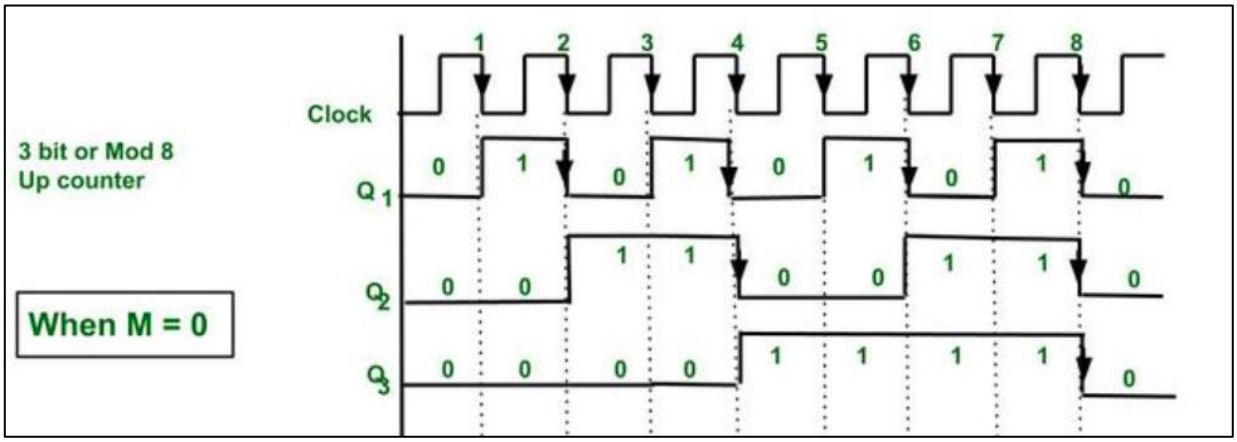
The 3-bit Synchronous binary up counter contains three T flip-flops & one 2-input AND gate. All these flip-flops are negative edge triggered and the outputs of flip-flops change affect synchronously. The T inputs of first, second and third flip-flops are 1, Q0 & Q1 Q0 respectively.

The output of first T flip-flop **toggles** for every negative edge of clock signal. The output of second T flip-flop toggles for every negative edge of clock signal if Q0 is 1. The output of third T flip-flop toggles for every negative edge of clock signal if both Q0 & Q1 are 1.

Truth Table:

State	Q_C	Q_B	Q_A
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

Timing diagram:



PROCEDURE: -

1. Connect the circuit as shown in figure.
2. Apply VCC & ground signal to the IC.
3. Apply various input data to the logic circuit.
4. Observe the input & output according to the truth table.

RESULT: - The 3-bit binary synchronous up counter is verified.

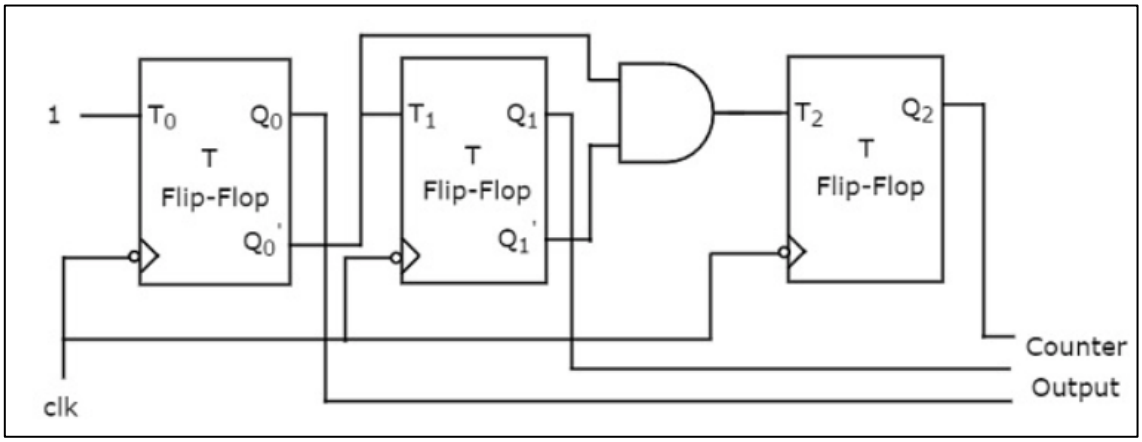
Practical-21

Aim: - To verify the working of Synchronous down Counter.

APPARATUS REQUIRED: Logic trainer kit, Flip-flop ICs-7400, 7404, 7410, Resistor 220Ω, Battery 9V, wires.

Synchronous down Counter

An 'N' bit Synchronous binary down counter consists of 'N' T flip-flops. It counts from $2^N - 1$ to 0. The **block diagram** of 3-bit Synchronous binary down counter is shown in the following figure.



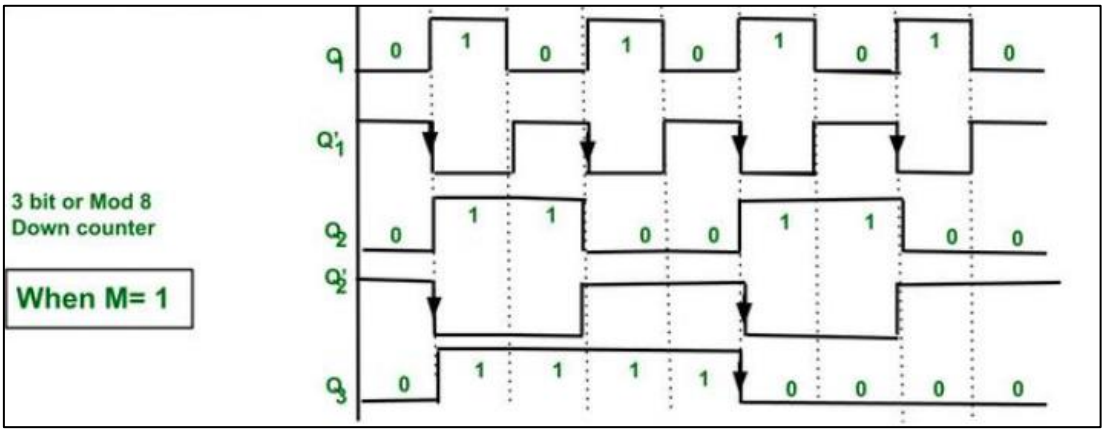
The 3-bit Synchronous binary down counter contains three T flip-flops & one 2-input AND gate. All these flip-flops are negative edge triggered and the outputs of flip-flops change affect synchronously. The T inputs of first, second and third flip-flops are 1, Q0 & Q1 Q0 respectively.

The output of first T flip-flop **toggles** for every negative edge of clock signal. The output of second T flip-flop toggles for every negative edge of clock signal if Q0 is 1. The output of third T flip-flop toggles for every negative edge of clock signal if both Q1& Q0 are 1.

Truth Table:

Counter State	Q_2	Q_1	Q_0
7	1	1	1
6	1	1	0
5	1	0	1
4	1	0	0
3	0	1	1
2	0	1	0
1	0	0	1
0	0	0	0

Timing diagram:



PROCEDURE: -

1. Connect the circuit as shown in figure.
2. Apply VCC & ground signal to the IC.
3. Apply various input data to the logic circuit.
4. Observe the input & output according to the truth table.

RESULT: - The 3-bit binary synchronous down counter is verified.

Practical-22

Aim: - To verify the working of Synchronous MOD-N Counter.

APPARATUS REQUIRED: Trainer Kit, IC 7490, IC 7400, and IC 7410, Patch chord.

Synchronous MOD-N Counter

The value of N can be different from power of 2. Also, the counting sequence may be random for example some cyclic code (8421, 2423 etc). The following method is applied for designing for mod N and any counting sequence.

Design for Mod-N counter: The steps for the design are –

Step 1: Decision for number of flip-flops –

Example: If we are designing mod N counter and n number of flip-flops are required then n can be found out by this equation.

$$N <= 2n$$

Here we are designing Mod-10 counter Therefore, N= 10 and number of Flip flops (n) required is

For n =3, 10<=8, which is false.

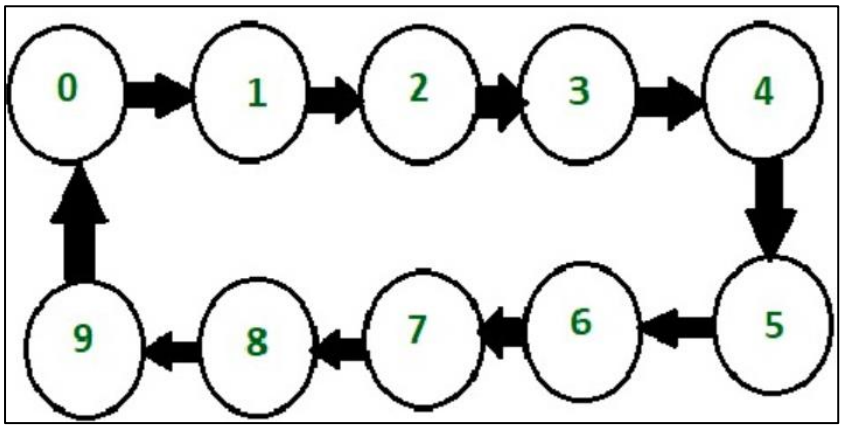
For n= 4, 10<=16, which is true.

Therefore number of FF required is 4 for Mod-10 counter.

Step 2: Write excitation table of Flip flops – Here T FF is used

Previous state(Q_n)	Next state(Q_{n+1})	T
0	0	0
0	1	1
1	0	1
1	1	0

Step 3: Draw state diagram and circuit excitation table –



A decade counter is called as mod -10 or divide by 10 counter. It counts from 0 to 9 and again reset to 0. It counts in natural binary sequence. Here 4 T Flip flops are used. It resets after Q3 Q2 Q1 Q0 = 1001.

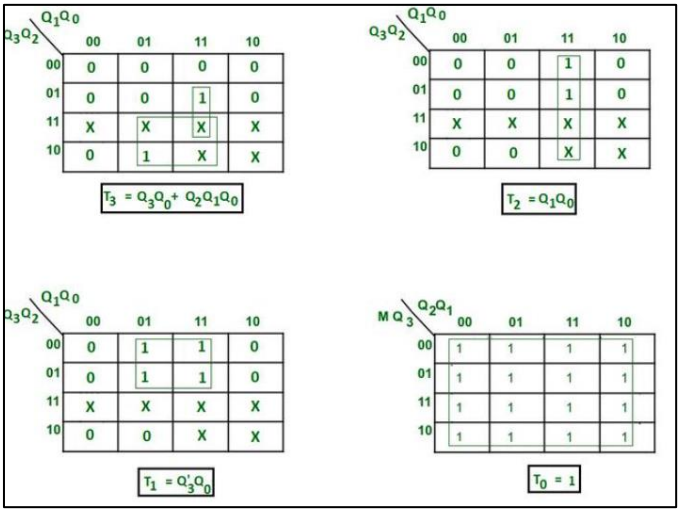
Circuit excitation table –

Here Q3 Q2 Q1 Q0 are present states of four flip-flops and Q*3 Q*2 Q*1 Q*0 are next counting state of 4 Flip flops. If there is a transition in current state i.e if Q3 value changes from 0 to 1 or 1 to 0 then there's corresponding T(toggle) bit is written as 1 otherwise 0.

Q_3	Q_2	Q_1	Q_0	Q^*_3	Q^*_2	Q^*_1	Q^*_0	T_3	T_2	T_1	T_0
0	0	0	0	0	0	0	1	0	0	0	1
0	0	0	1	0	0	1	0	0	0	1	1
0	0	1	0	0	0	1	1	0	0	0	1
0	0	1	1	0	1	0	0	0	1	1	1
0	1	0	0	0	1	0	1	0	0	0	1
0	1	0	1	0	1	1	0	0	0	1	1
0	1	1	0	0	1	1	1	0	0	0	1
0	1	1	1	1	0	0	0	1	1	1	1
1	0	0	0	1	0	0	1	0	0	0	1
1	0	0	1	0	0	0	0	1	0	0	1

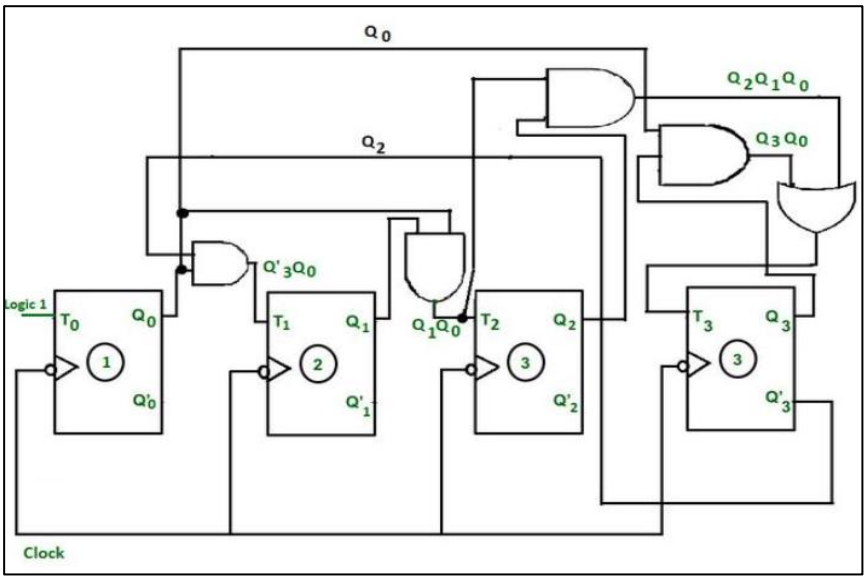
Step 4: Create Karnaugh map for each FF input in terms of flip-flop outputs as the input variable –

Simplify the K map –

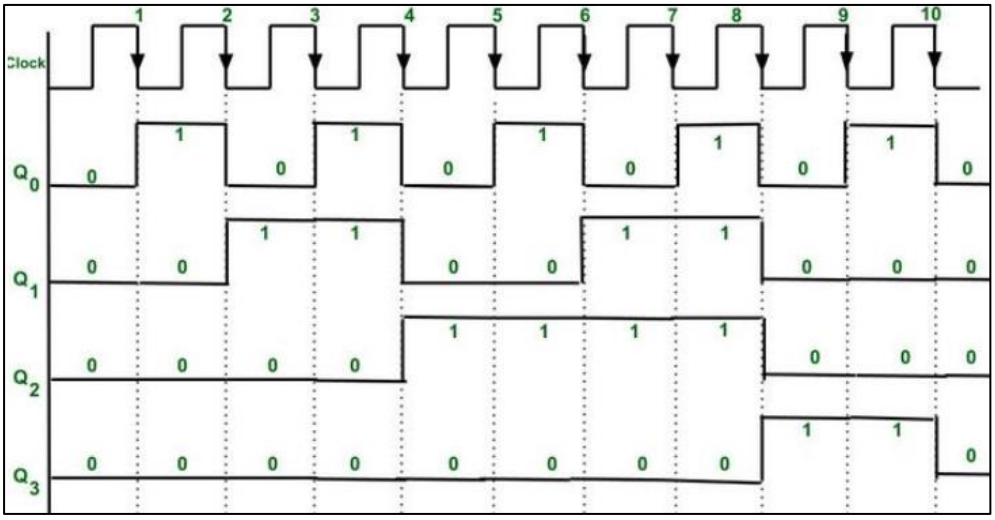


Step 5: Create circuit diagram –

- Here negative edge triggered clock is used for toggling purpose.
- The clock is provided to every Flip flop at same instant of time.
- The toggle (T) input is provided to every Flip flop according to the simplified equation of K map.



The state of a FF will change only when toggle input (T) of a FF is 1.



Explanation:

- Initially Q3 Q2 Q1 Q0 are 0 0 0 0.
- The sequence of counter can be verified from the timing diagram. At every falling edge of the clock output Q0 toggles because T0 is connected to logic 1.
- T1 becomes 1 only when expression T1 = Q'3Q0 becomes 1 also if clock falling edge occurs (because there is negative edge triggering) then the output state of T1 i.e Q1 will change.
- T2 becomes 1 only when expression T2 = Q1Q0 becomes 1 also if clock falling edge occurs then the output state Q2 will change.
- T3 becomes 1 only when expression T1 = Q3Q0 + Q2Q1Q0 resultant becomes 1 also if clock falling edge occurs (because there is negative edge triggering) then the state of Q3 will change.
- We get Output as Q3 (MSB) Q2 Q1 Q0 (LSB).
- After 10th falling edge the output state of all the FFs again becomes 0 0 0 0.

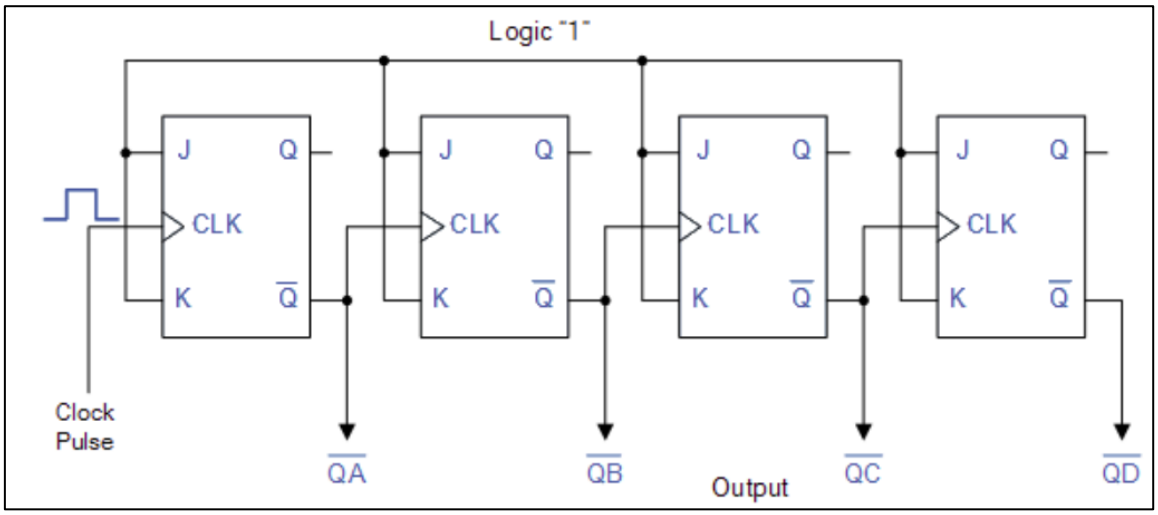
Practical-23

Aim: - To verify the working of Asynchronous Bidirectional Counter.

APPARATUS REQUIRED: Integrated Circuits (ICs) - Flip-flops (e.g., D Flip-flops, JK Flip-flops) Logic Gates (e.g., AND, OR, NOT gates) Power Supply, Breadboard, Connecting Wires Oscilloscope or Logic Analyzer (for verifying results)

Asynchronous Bidirectional Counter

An asynchronous bidirectional counter is a digital electronic circuit that counts both up and down, depending on the input signals. This type of counter is often used in various applications where both incrementing and decrementing of a count are required.



Procedure:

Design the Circuit: Design the asynchronous bidirectional counter using flip-flops and logic gates. You can use D flip-flops or JK flip-flops depending on your preference.

Implement the Circuit: Connect the components on the breadboard according to the designed circuit diagram. Ensure proper power connections.

Input Signals: Provide two input signals: UP and DOWN. These signals will control the counting direction of the counter. You can use toggle switches to manually control these signals.

Clock Signal: Provide a clock signal to the flip-flops. This clock signal will determine the speed of counting. You can use a function generator or a simple oscillator circuit to generate a clock signal.

Verify Counting: Apply the UP and DOWN signals to the counter and observe the counting sequence. Ensure that the counter counts up when the UP signal is active and counts down when the DOWN signal is active.

Test with Different Inputs: Test the counter with different combinations of UP and DOWN signals to verify its bidirectional counting capability.

Measure Timing: Use an oscilloscope or logic analyser to measure the timing characteristics of the counter. Ensure that the timing requirements are met for proper operation.

Verify Results: Compare the observed counting sequence with the expected sequence based on the input signals. Verify that the counter behaves as expected in both counting up and counting down modes.

Result:

- The asynchronous bidirectional counter should successfully count up and down based on the input signals (UP and DOWN).
- The counting sequence should match the expected sequence.
- The counter should operate reliably within the specified timing parameters.

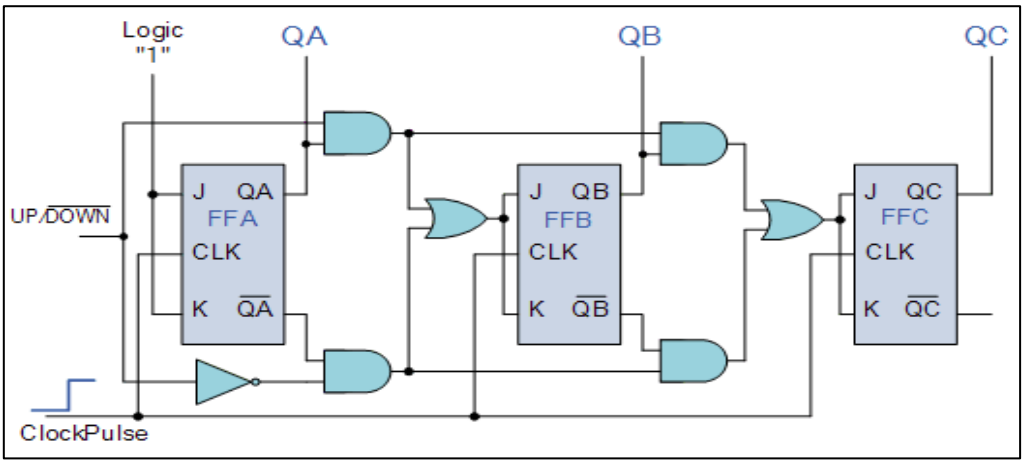
Practical-24

Aim: - To verify the working of Synchronous Bidirectional Counter.

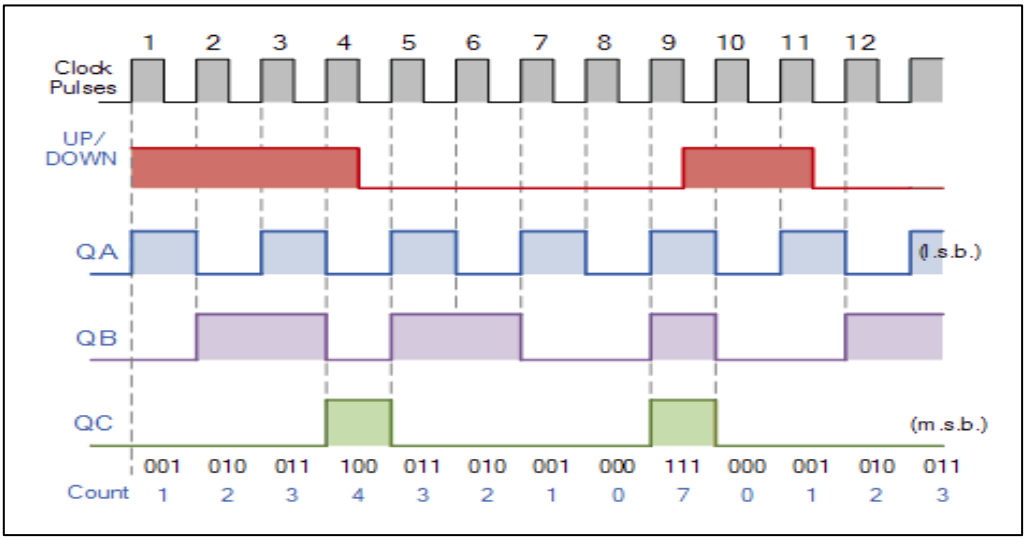
APPARATUS REQUIRED: Integrated Circuits (ICs) such as 74LS193 or 74LS169 (These are 4-bit synchronous up/down binary counters), Breadboard, Power supply (typically +5V), LEDs (Light Emitting Diodes) Resistors, Push-button switches, Connecting wires

Synchronous Bidirectional Counter

A synchronous bidirectional counter is a digital circuit that counts both upwards and downwards based on the input signals provided. Here's how you can build and verify the working of a synchronous bidirectional counter along with the required apparatus, procedure, and explanation.



Timing diagram:



Procedure:

1. Connect the power supply to the breadboard.
2. Insert the ICs (74LS193 or similar) into the breadboard.
3. Connect the VCC (+5V) and GND pins of the ICs to the power supply.
4. Connect LEDs to the output pins of the counter (Q0-Q3) to observe the count.
5. Connect push-button switches to the UP, DOWN, and Clock input pins.
6. Apply a clock signal to the Clock input. You can generate this signal using a function generator or manually by pressing a push-button.
7. Press the UP or DOWN button to change the count direction.

8. Observe the LEDs to verify the count.

Results:

1. The counter should count up by one when the UP (S) input is activated and the clock signal pulses.
2. The counter should count down by one when the DOWN (R) input is activated and the clock signal pulses.
3. The counter should alternate between incrementing and decrementing when both UP and DOWN inputs are activated alternately.
4. The LEDs connected to the output pins (OUT0 to OUT3) should indicate the current count value in binary.
5. The oscilloscope should show a stable clock signal and the appropriate transitions on the counter's output pins.